Образовательные технологии проектирования цифровых систем на кристаллах в учебном процессе ХНУРЭ

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IEEE Computer Society Golden Core Member

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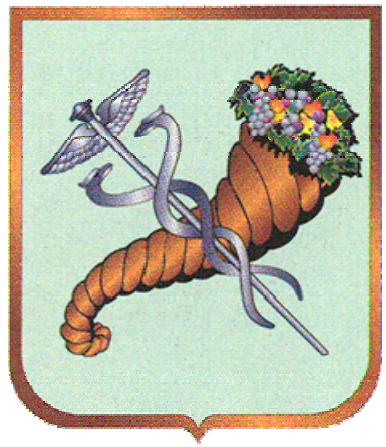
Agenda

- Education in Kharkov
- University Faculties
- Companies – our partners for education and working
- Our projects
- Club's Education
- East-West Design & Test Symposium 2007
- Educational projects
- What we are waiting from IT-industry and Cadence

Kharkov

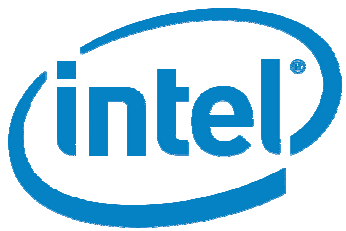


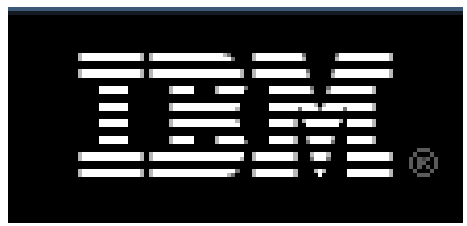
- Population: **1.5 millions**
- Science and education center
  - 60 research institutes
  - 30 higher education institutes
  - 80 libraries
  - 655.1 thousands of pupils, including 280000 students
  - 3915 PhD students
  - 1700 doctors of science
  - Students from 90 countries
  - 160 specialties
  - 12 of 73 objects, which are national patrimony of Ukraine, are located in Kharkov
  - Kharkov is scientific and educational leader of Ukraine.
- Unemployed: 44.3 thousands people

Kharkov National University of Radio Electronics

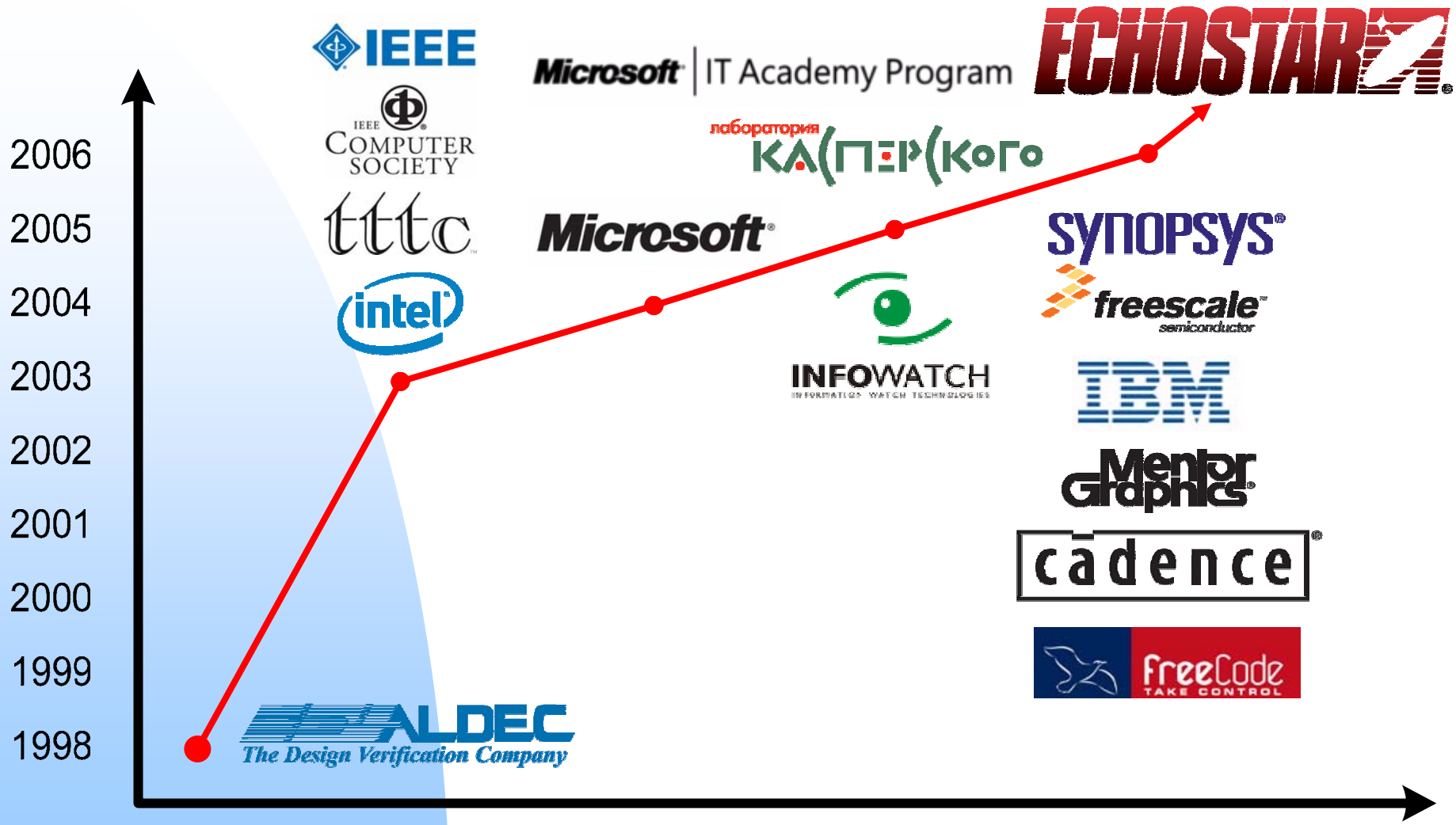
- Kharkov National University of Radio Electronics was founded 75 years ago.
- It was one of the best University in USSR in 70th - 90th in the field of Radio electronics. Today the University is the leader among all technical universities of Ukraine.
- Total number of students is more than 12000, 150 professors and doctors of science.
- 500 PhD and professor assistants work in the University.
- Technical equipment of laboratories is more than 1200 computers. The students of our University acquire professions which are required not only in Ukraine but in other countries also.
- Graduate students of our University work in USA, Germany, England, Finland, France, Poland as well.
- The University consists of 7 faculties. The faculty of Computer Engineering and Control is one of the best not only in the university but among other technical universities, which have similar specialties.

World leading companies manage Computer Engineering Faculty





History of brands contacts




Faculties in KNURE


- **FACULTY OF COMPUTER ENGINEERING AND CONTROL** – Dean Prof. Hahanov Vladimir Ivanovich (1654 students)
- **Faculty of Computer Sciences** – Dean Prof. Mashtalir Vladimir Petrovich (1651 students)
- **Faculty of Applied Mathematics and Management** – Dean Prof. Doroshenko Volodymyr Oleksiyovich (822 students)
- **Faculty of Radio Engineering** – Dean Prof. Sakalo Serguei Nikolaevich (675 students)
- **Faculty of Telecommunication Systems** – Dean Prof. Popovsky V.V. (986 students)
- **Faculty of electronic devices** – Dean Prof. Filipenko Alexander Ivanovich (775 students)
- **Faculty of electronic engneering** – Dean Prof. Alexandrov Yuri Nikolaevich (558 students)

Computer Engineering Faculty

Number of students: 1654;

Number of employees: 154 сотрудника;

Number of teachers 120 (77 PhDs, 15 Dr of Sciences);

6 laboratories and more than 300 PC stations,

6 offices from local and brand industries - Aldec, Kaspersky Lab, Freecode, Softline, Institute of Information Technology, ADB, Echostar is coming**.**

More than 300 foreign students from 12 countries studying in English.

Departments:

- **CAD Department – 21 employees (Specialized Computer Systems),**
- **Computer Systems Department – 65 employees (Computer Systems and Networks, System, Programming),**
- **Information Technology Security – 26 employees (Information Security in Computer Systems and Networks).**

Others specialties:

- **Control Systems and Automation**
- **Flexible Computer Systems in Robotics**
- **Wireless Computer Systems and Networks**

KNURE rate for today

KNURE is the first University in Ukraine in area of Radio Electronics.

KNURE is the 31st University in Ukraine among 200 Universities.

According to Ukraine Universities rate, Kharkov National University of Radio Electronics has 6 rank from list of Technical Universities (total number is 30):

Kiev Polytechnic University
- **Kharkov Polytechnic University**
- **Kharkov Aerospace University – 59 Raitio**
- **Asov Technical University**
- **Lviv Polytechnic University**
- **Kharkov National University of RadioElectronics**

50 Universities – Partners of CAD-dept.

Yerevan University

Saratov State University

Nizhny Novgorod University

Tallinn University of Technology

Warsaw University of Technology

Purdue University

Rennes University

Sophia University

Las Vegas University

Turino University of Technology

Bialystok University

Dresden University of Technology

Bielorussia University of RadioTechnics

30 Ukrainian Universities - Partners of CAD-dept.

Moscow Institute of Control Sciences

Kharkov National Aerospace University

Donetsk National Technical University

Kharkov State Academy of Culture

Odessa National Polytechnic University

Kharkov National Polytechnic University

Odessa National University Named after Mechnikov

Kharkov National Academy of Railway Transport

Cherkassy State University

Kharkov Polytechnic University

Special HW/SW courses in KNURE

- CE039 Computer electronics 4 ECTS
- CE001 Computer circuit design 6 ECTS
- CE002 Computer architectures 6 ECTS
- CE003 System programming 6 ECTS
- CE005 System software 6 ECTS
- CE015 Specialized microprocessor systems design 4 ECTS
- CE044 Computer systems and networks information security 3 ECTS
- CE008 Logic simulation 4 ECTS
- CE011 PLD Design Automation Methods 4,5 ECTS
- CE002 OBJECT-ORIENTED PROGRAMMING 3 ECTS
- CE007 HARDWARE DESCRIPTION LANGUAGES 3 ECTS
- CE012 BASIS OF COMPUTER DIAGNOSTICS
- CE013 SPECIALIZED COMPUTER SYSTEM ARCHITECTURES
- CE014 MICROPROCESSOR TECHNOLOGY (SPECIALISED COMPUTER SYSTEMS)
- CE005 OPERATING SYSTEM
- CE006 TEXT AND GRAPHIC EDITORS (Specialized Computer Systems)
- CE002 OBJECT-ORIENTED PROGRAMMING 3 ECTS
- CE041 PARALLEL AND DISTRIBUTED COMPUTING 3 ECTS
- CE042 COMPUTER SYSTEMS 5 ECTS
- CE043 COMPUTER NETWORKS 5 ECTS
- CE004 COMPUTER SYSTEMS DESIGN AUTOMATION 3 ECTS
- CS002 DATABASE ORGANIZATION AND DATA PROCESSING 3 ECTS

HW/SW RF and TV courses in KNURE

- HW/SW Design and Testing
  - Design Automation, 156 hours
  - HDL Languages (VHDL, Verilog, System C), 156 hours
  - SW languages (C++, C#, Jawa, .Net), 156 hours
  - Technology and CAD Tools, 108 hours
  - Digital Systems Testing and Testable Design , 156 hours
- RF/Analog design
  - Computer Aided A/RF-Design, 162 hours
  - Computer RF/A simulation, 162 hours
- Digital TV
  - Television standards and record formats, 216 hours
  - Digital recording and playback devices, 108 hours
  - DSP, 108 hours

Conferences, organized by KNURE

- IEEE East- West Design & Test Conference
- International Workshop “Information technologies to Science and Education”
- Microsoft Academic Days
- Kaspersky Workshop
- International Radioelectronics Forum
- International Youth Conference “Radio Electronics and Youth in the XXI Century”
- Education and Virtuality
- International Conference on physics of Laser Crystals
- International Conference on Precision Oscillations
- International Conference on Navigation and Location systems
- International Conference on Telecommunication technologies and Networks
- International Conference on Information systems and Technologies
- International Conference on Optoelectronics
- International Conference on Microelectronics and Nanotechnology
- International Conference on Electromagnetic Compatibility and Survivability

«Intel Technologies School of Multicore»

3-12 мая 2007 года

- **Харьковский Национальный Университет радиоэлектроники**
- **Проводится по инициативе и при поддержке компании Intel совместно с университетами Харькова, Нижнего Новгорода, Ростова-на-Дону, Таганрога**
- **Программа** Technologies School of Multicore**:**
- 1) Архитектура Intel Core 2 Duo;Intel tools: Compiler, VTune, MKL, IPP, Thread checker, Thread Profiler;Программирование PThreads, OpenMP;Масштабируемость многопоточных приложений.
- **Темы тренинга:**Введение в высокопроизводительные вычисления, средства программирования для параллельных вычислительных систем, параллельные алгоритмы в моделировании физических явлений и визуализации данных в реальном масштабе времени, система MC# как язык для многопоточного программирования на мультиядерных процессорах, технологии параллельного программирования, мастер-класс по Grid-технологиям.Занятия проводятся сотрудниками компании Intel и участниками конкурса Intel по обновлению учебно-методических материалов, посвященных программированию на многоядерных архитектурах.
- **Организационный комитет:** Нижний Новгород: (8312) 16-24-91,
- Фадина Лариса Михайловна,
- Харьков: (8057) 70-21-326, Хаханов Владимир Иванович

Awards of students.1

- IEEE Recognition Award
- IEEE Gerald W. Gordon Award
- Diploma for Best Scientific Project in CAD Projects contest by Intel 2003
- Diploma of Ukrainian Ministry of Science and Education for the Best Systems Program
- Diploma of Ukrainian Ministry of Science and Education in nomination “For professionalism”
- Diploma for the Best Student’s Application
- Diploma for “Mobile Games Development Kit” in J2ME contest by Sun Microsystems
- 14 Diplomas for student Olympiads

Awards of students.2

- Diploma of the 1st place winner in Ukrainian Olympiad on Digital Systems Testing, 2006
- Diploma of the 3rd place winner in Microsoft Imagine Cup, 2006
- Diploma of the best scientist nomination in Concourse of Kharkov Citizen, 2006
- Diploma of IEEE Computer Society Golden Core Member, 2006
- EWDT Sponsorship by Microsoft, 2006
- EWDT Sponsorship by Intel, 2006
- EWDT Sponsorship by Cadence, 2006

Scientific results of CAD department

- 86 published papers including 5 – in foreign journals; 49 – conferences out of USSR, 2006
- 14 students and professors are attended in international fairs, 2006
- 32 international program and grants, 2005
- 24 Diplomas in area of IT-science and technology, 2005, 2006
- 12 TV air translation devoted achievement of our team, 2006, 2 TV for the current Year
- 7 dissertations including Doctor of Science prepared for defense in 2007

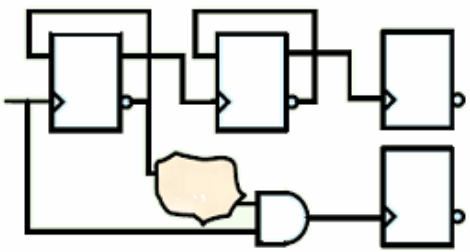
Projects

- **SIGETEST-** *fault simulation and test generation for complex digital devices*
- **PRUS -** *programmable unlimited systems, spherical multiprocessor for Boolean equations solving*
- **Independent Test Lab:**
  - **INFOWATCH Mail Storage**
  - **Kaspersky Antivirus**
- **HES+ARM Board -** *HW/SW co-simulator for complex SoCs verification*
- **Assertions Engine -** *temporal assertions checker*
- **CORDIC -** *IP Core generator for fast calculations of trigonometric functions in hardware*
- **JPEG/MPEG4 – SoC implementation (R&D)**
- **OpenTEST -** *Knowledge testing computer system*
- **ASFTEST -** *automatic test synthesis system for state machines*
- **eXCite Tool Testing**
- **LAN Analyzer based on Novell ZEN MS, Norway**

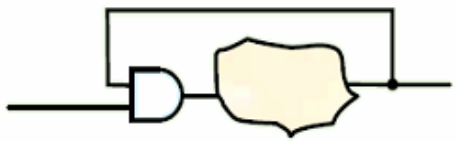
LINT – СИСТЕМА ДИАГНОСТИРОВАНИЯ HDL-ПРОЕКТОВ

- Мотивация определяется тремя основными проблемами при разработке аппаратуры: 1) Высокая стоимость (до 1000000 долларов) исправления ошибок на поздних стадиях проектирования цифровых систем; 2) Менеджмент и координация командной разработки сверхсложных проектов; 3) Уменьшение интервала времени для выхода готового продукта на рынок электронных технологий.
- Цель предложенной разработки – минимизация материальных затрат и времени проектирования сверхсложных (более 1 000 000 вентилей) цифровых систем на кристаллах за счет использования программного комплекса автоматизированного диагностирования функциональных неисправностей на ранних стадиях проектирования. Отличительная особенность – используется lint-технология, реализующая библиотеку стандартных и оптимальных решений от мировых производителей SoC в процессе создания кода, инвариантного к стандартам и маршрутам проектирования ведущих EDA-компаний мира.
- Функциональности LINT- системы диагностирования: 1) Сканирование исходного HDL-кода для создания внутренней модели проекта; 2) Анализ модели в целях диагностирования функциональных (семантических) несоответствий относительно заданных правил и шаблонов; 3) Верификация валидной синтезируемости конструкций RTL-модели в целях обеспечения ее полного соответствия с пост-синтезной моделью вентильного уровня; 4) Поддержка IEEE-стандартов тестопригодного проектирования; 5) Семантическая проверка test bench, как кода, дополняющего проект.
- Научная новизна – впервые предложена универсальная модель диагностирования функциональных неисправностей на ранних стадиях проектирования и модель поиска шаблонов диагностирования сложных правил проектирования, не проверяемых конкурентами.
- Рыночная привлекательность: 10000 инсталляций в США, Азии, Европе. LINT-система диагностирования работает под управлением ОС Windows, LINUX/UNIX, SUN. Конкуренты (Synopsis LEDA, Atrenta Spyglass, TransEDA Vn-Check) имеют аналогичные средства, ориентированные только для ОС LINUX и SUN.

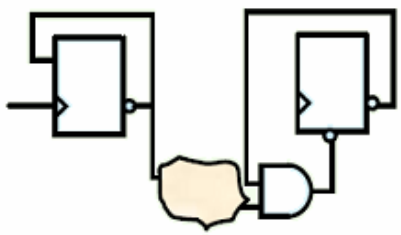
Riviera LINT: fresh approach to RTL design rules checking



Avoid generation of asynchronous clocks inside a circuit



Avoid feedback of combinational circuits



Avoid feedback that spans asynchronous reset

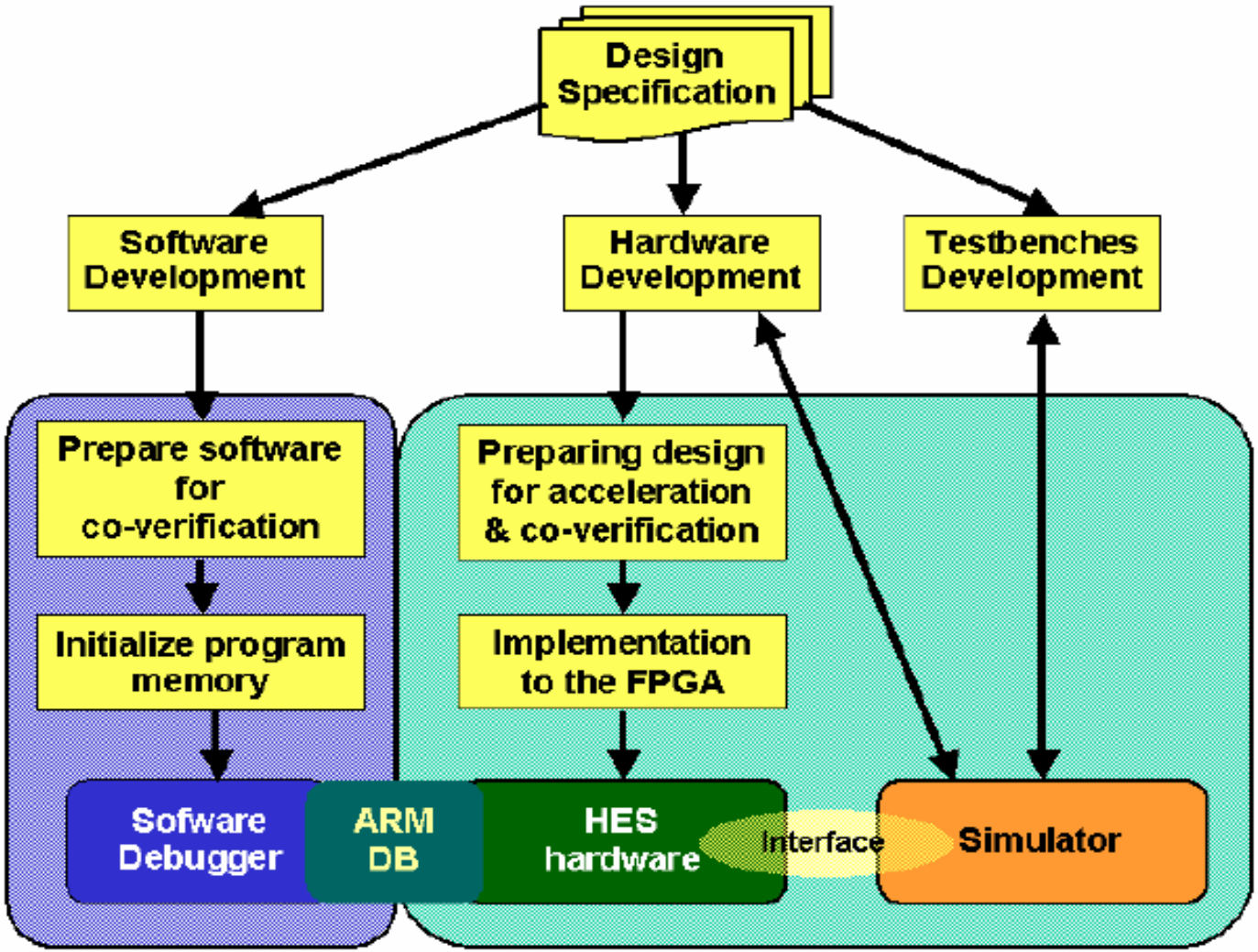
Patterns recognition on synthesized netlist:

- combinational loops
- mixing feedbacks and asynchronous controls
- clock tree / initial reset tree distribution
- Design-For-Test constraints
- gated clocks

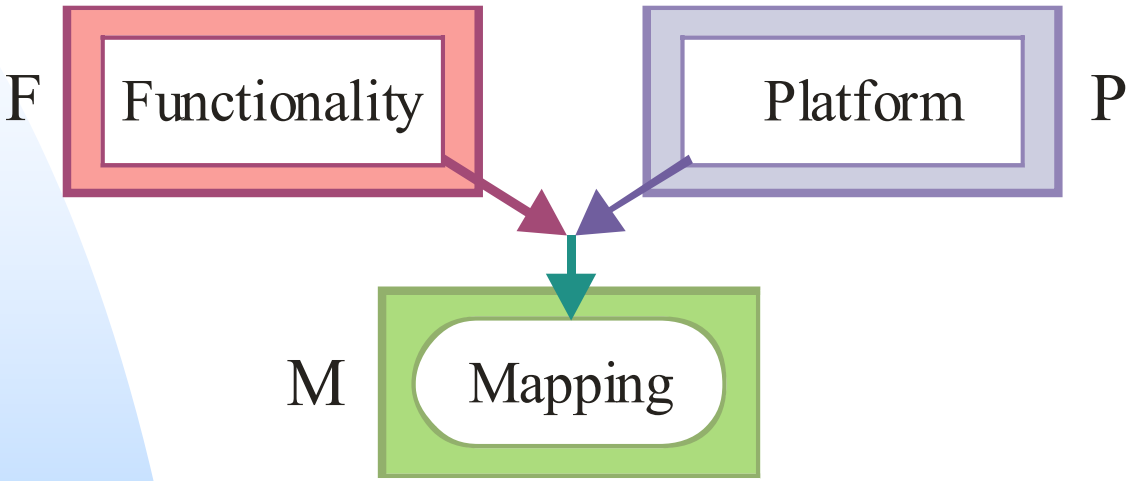
Powerful configurability features:

- Configuration files with settings
- Rulesets / Policies
- Parameterization of existing rules
- Embedded pragmas for in-place errors masking
- C++ API for custom user-defined rules

Design Flow


Design Specification
Software Development
Hardware Development
Testbenches Development
Prepare software for co-verification
Initialize program memory
Preparing design for acceleration & co-verification
Implementation to the FPGA
Sofware Debugger
ARM DB
HES hardware
Interface
Simulator

Electronic system-level design tools.
Platform-based design classification framework elements

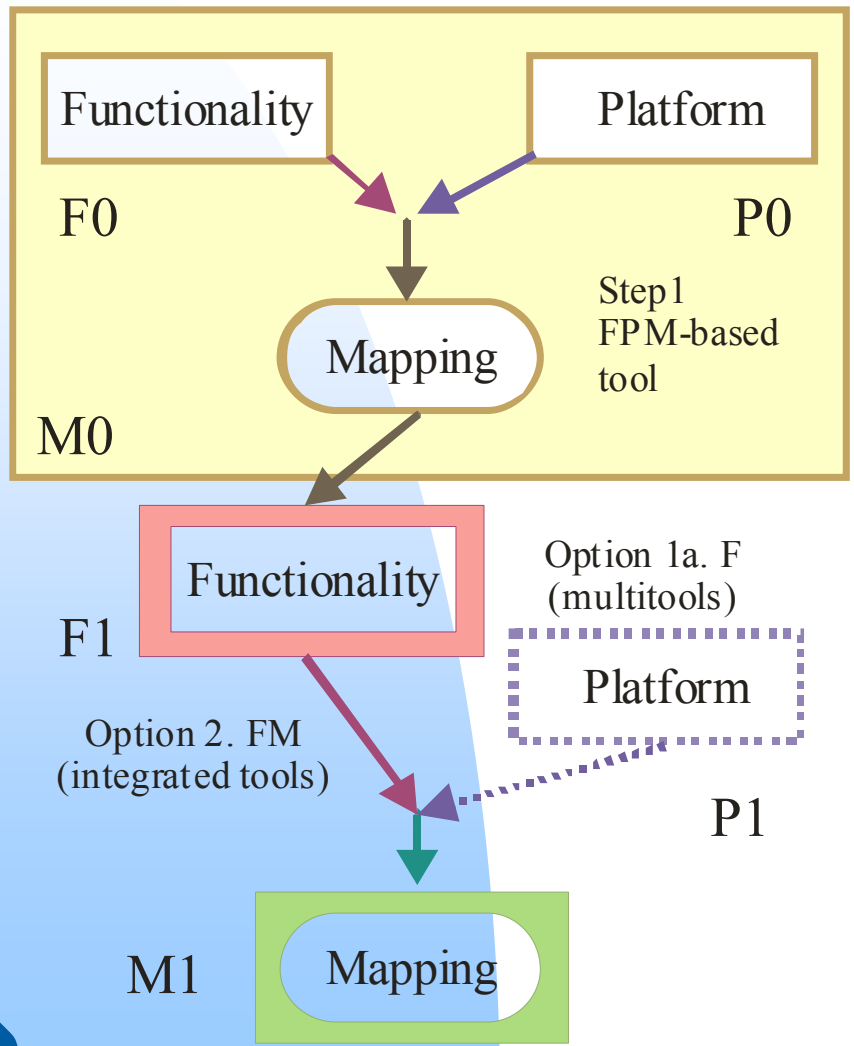


- *Functionality* indicates functional representations of a design completely independent of implementations architecture.
- *Platform* concerns the modules used to implement the functional description – for example, processors, memories, and custom hardware.
- *Mapping* refers to instances of the design in which the functionality has been assigned to a set of correctly interconnected modules.

Abstraction levels

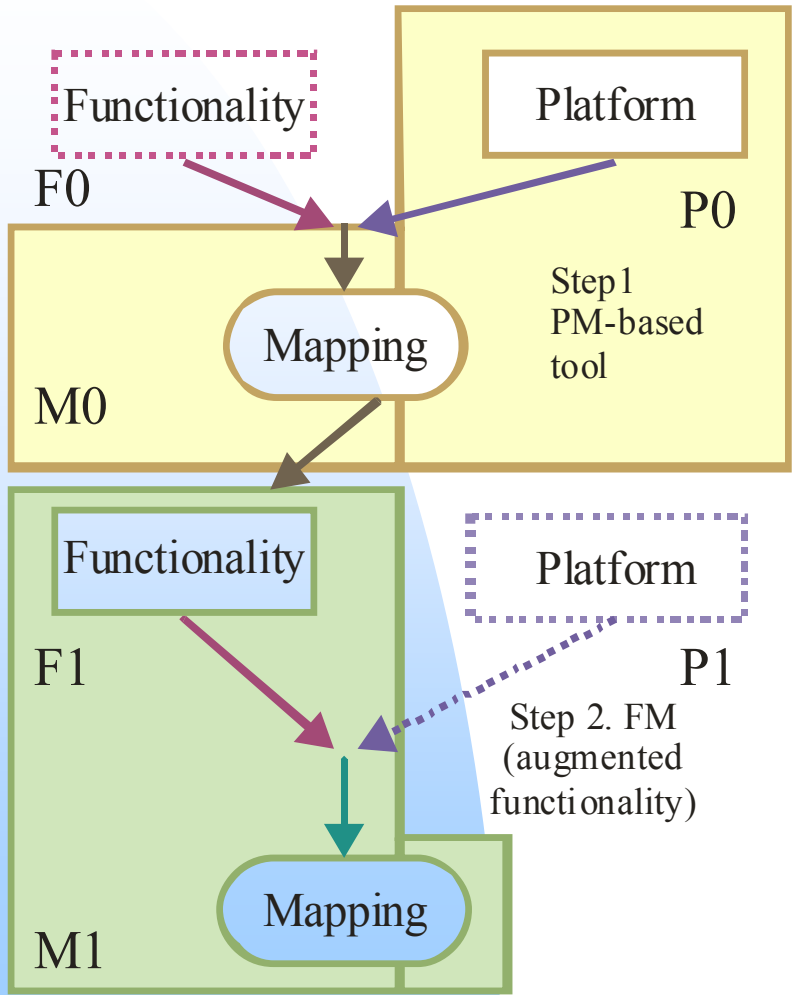
- *System level S* correspond to heterogeneous designs that use different models of computation (MoCs) to represent function, platform, and mappings.
- *Component level C* involves subsystems containing homogeneous components.
- *Implementation level I* comprises the final design step, when the design team considers the job complete.

Scenario 1: New application design from specification



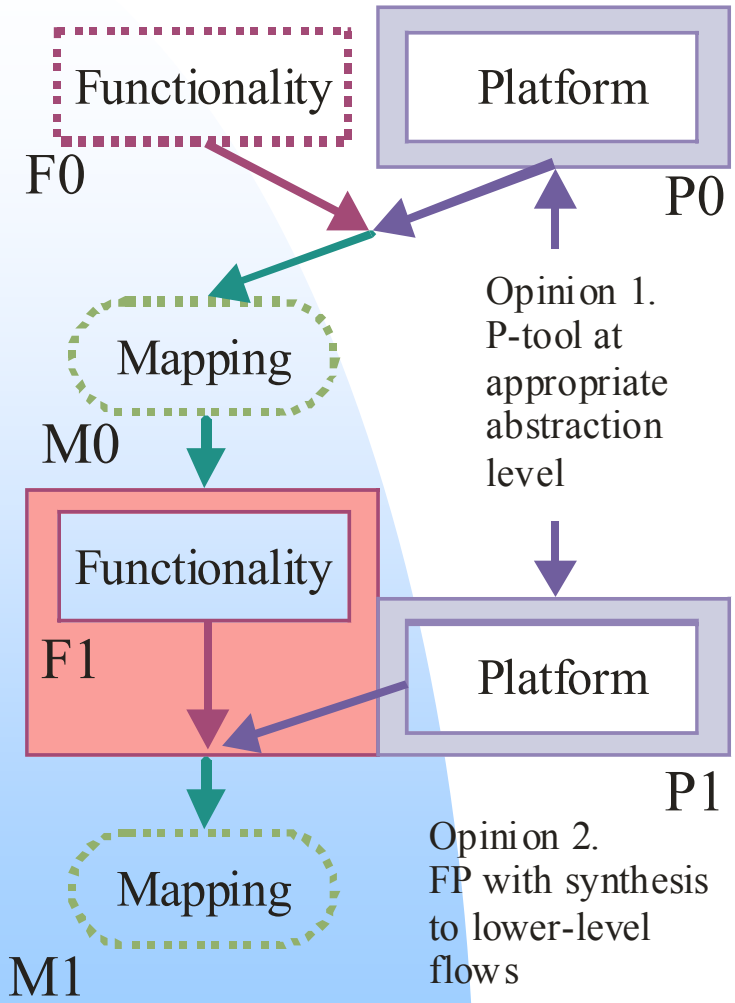
- The requirements of this scenario include the need to start from high-level specification; the desire to capture and modify the initial specification quickly, the ability to express concurrency, constraints and other behavior-specific characteristics efficiently; and the ability to capture useful abstract services for implementing high-level specifications into a more detailed functional view.

Scenario 2: New integration platform development



- This scenario describes the development of a new integration platform: a hardware architecture, embedded-software architecture, design methodologies (authoring and integration), design guidelines and modeling standards, virtual-components characterization and support, and design verification, focusing on a particular target application.

Scenario 3 Legacy design integration



- The scenario represents a common situation for many companies wishing to integrate their existing designs into new ESL flows

Table 1. Tools in bin F: Industrial.(C: component level; I: Implementation level; S:system level			
Tools	Focus	Abstraction	Web site
Matlab	High-level technical computing language and interactive environment for algorithm development, data visualization, analysis, and numerics computation	S: Matlab language, vector, and matrix operations	http://www.mathworks.com/products/matlab
Scicos	Graphically model, compile, and simulate dynamic systems	S: Hybrid systems	http://www.scilab.org
Verdi	Debugging for System Verilog	I: Discrete event	http://www.novas.com
SystemVision	Mixed-signal and high-level simulation	S:VHDL-AMS, Spice, C	http://www.mentor.com/products/sm/systemvision
EDAStar	Military and aerospace system-level design	S: Performance models	http://www.edaptive.com
DBRover, TemporalRover, StateRover	Temporal rules checking, pattern recording, and knowledge reasoning	C: Statecharts assertions	http://www.time-rover.com
Maple	Mathematical problem devolopment and solving	S: Mathematical equations	http://www.maplesoft.com
Mathematica	Graphical mathematical development and problem solving with support for Java, C, and Net	S: Mathematical equations	http://www.wolfram.com
CSIM 19	Process-oriented, general-purpose simulation toolkit for C and C++	S: C. C++	http://www.mesquite.com
Agilent Ptolemy	Functional verification	C: Timed synchronous dataflow	http://www.agilent.com
LabView	Test, measurement, and control application development	S: LabView programming language	http://www.ni.com/labview

Table. Tools in bin P: Industrial.

Provider	Tools	Focus	Abstraction	Web site
Prosilog	Nepsys	Standards-based IP libraries and support tools (SystemC)	C: RTL and transaction-level SystemC, VHDL for SoCs	http://www.prosilog.com
Beach Solutions	EASI-Studio	Solutions to package and deploy IP in a repeatable, reliable manner	C: Interconnection	http://www.beachsolutions.com
Altera	Quatrus II	FPGAs, CPLDs, and structured ASICs	I: IP blocks, C, and RTL; FPGAs	http://www.altera.com
Xilinx	Platform Studio	IP integration framework	C: IP blocks, FPGAs	http://www.xilinx.com
Mentor Graphics	Nucleus	Family of real time operating systems and development tools	S: Software	http://www.mentor.com/products/embedded_software/nucleus_rtos
Sonics	Sonics Studio	On-chip interconnection infrastructure	I: Bus-functional models	http: sonicsinc.com
Xilinx	ISE, EDK, XtremeDSP	FPGAs, CPLDs, and structured ASICs	I: IP blocks, C, and RTL; FPGAs	http://www.xilinx.com
Design and Reuse	Hosted Extranet Services	IP delivery systems	S: All types of IP	http://www.design-reuse.com
Stretch	Software Configurable Processor compiler	Compile a subset of C into hardware for instruction extensions	C: Software-configurable processors	http://www.stretchinc.com
ProDesign	CHIPit	Transaction-based verification platform	C: FPGA-based rapid prototyping	http://www.prodesign-usa.com

Table. Tools in bin P: Industrial.

Provider	Tools	Focus	Abstraction	Web site
Mathworks	Real-Time Workshop	Code-generation and embedded-software design	S: Simulink-level models	http://www.mathworks.com
dSpace	TargetLink	Optimized code generation and software development	S: Simulink models	http://www.dspace.com
ETAS	Ascet	Modeling, algorithm design, code generation, and software development, with emphasis on the automotive market	S: Ascet models	http://en.etasgroup.com/products/ascet/index.shtml
Yexploration	eXCite	Take virtually unrestricted ISO or ANSI-C with channel I/O behavior and generate Verilog or VHDL RTL output for logic synthesis	S: C language input	http://www.yxi.com
AccelChip	AccelChip and AccelWare	DSP synthesis; Matlab to RTL	C: Matlab	http://www.accelchip.com
Forte Design Systems	Cynthesizer System Center	Behavioral synthesis	C:SystemC to RTL	http://www.forteds.com
Future Design Automation	Co-development Suite	ASCI-C to RTL synthesis toolset	C: C to RTL	http://www.future-da.com
Catalytic	DeltaFX, RMS	Synthesis of DSP algorithms on processors or ASICs	I: Matlab algorithms	http://www.catalytic-inc.com
ACE Associate Compiler Experts	CoSu	Automatic generation of compilers for DSPs	I: DSP-C and embedded-C language extensions	http://www.ace.nl
Tenison	VTOC	RTL to C++ or SystemC	I: RTL, transactional	http://www.tenison.com

Table. Tools in bin FP: Industrial.

Provider	Tools	Focus	Abstraction	Web site
Mathworks	Simulink, State Flow	Modeling, algorithm design, and software development	S: Timed dataflow, FSM	http://www.mathworks.com

Table. Tools in bin FM: Industrial.

Provider	Tools	Focus	Abstraction	Web site
Celoxica	DK Design Suite, Agility Compiler, Nexus-PDK	Algorithmic design entry, behavioral design, simulation, and synthesis	C: Handle-C based	http://www.celoxica.com
Blue Spec	BlueSpec Compiler, BlueSpec Simulator	BlueSpec SystemVerilog rules and libraries	S: SystemVerilog and term-rewriting synthesis	http://www.bluespec.com
I-Logix	Rhapsody and Statemate	Real-time UML-embedded applications	S: UML based	http://www.ilogix.com
Menthor Graphics	Catapult C	C++ to RTL synthesis	C:Untimed C++	http://www.mentor.com
Esterel Technologies	SCADE, Esterel, Studio	Code generation for safety-critical applications such as avionics and automotive	I: Synchronous	http://www.esterel-technologies.com
Calypto	SLEC System	Functional verification between system level and RTL	C: SystemC, RTL	http://www.calypto.com

Table. Tools in bin PM: Industrial.

Provider	Tools	Focus	Abstraction	Web site
ARM	RealView MaxSim	Embedded microprocessors and development tools; system-level development tools	C: C++ ARM processor development	http://www.arm.com
Tensilica	Xtensa, XPRES	Programmable solutions with specialized Xlensa processor description from native C and C++ code	C: Custom ISA processor, C and C++ code	http://www.tensilica.com
Summit	System Architect, Visual Elite	Efficiently design and analysis the architecture and implementation of multicore SoCs and large-scale system	C: SystemC	http://www.sd.com
VaST Systems Technology	Comet, Meteor	Very high-performance processor and architecture models	processor, bus, and peripheral devices	http://www.vastsystems.com
Virtio	Virtio Virtual Platform	High-performance software model of a complete system	I: Vitual platform models at SystemC level	http://www.virtio.com

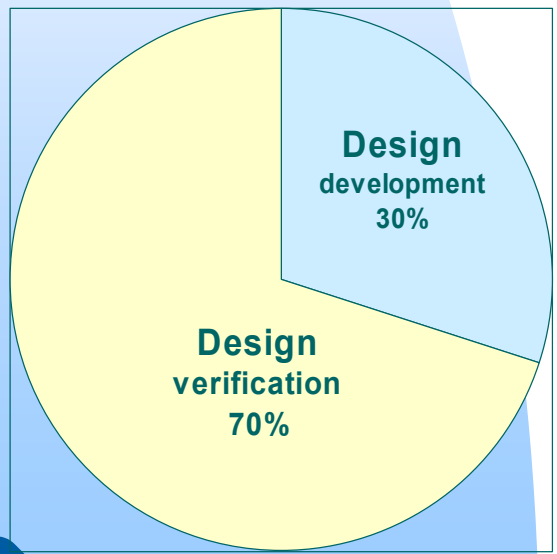
Table. Tools in metabin FPM: Industrial.

Provider	Tools	Focus	Abstraction	Web site
CoFluent Design	CoFluent Studio	Design space exploration through Y-chart modeling of functional and architectural models	S: Transaction-level SystemC	http://www.cofluentdesign.com
MLDesign Technologies	MLDesigner	Inegrated platform for modeling and analyzing the architecture, function, and performance of high-level system designs	S: Discrete event, dynamic dataflow, and synchronous dataflow	http://www.mldesigner.com
Mirabills Design	VisualSim product family	Multidomain simulation kernel and extensive modeling library	S: Discrete event, synchronous dataflow, continuous time, and FSM	http://www.mirabilisdesign.com
Synopsys	System Studio	Algorithm and architecture capture, performance evaluation	S:SystemC	http://www.synopsys.com

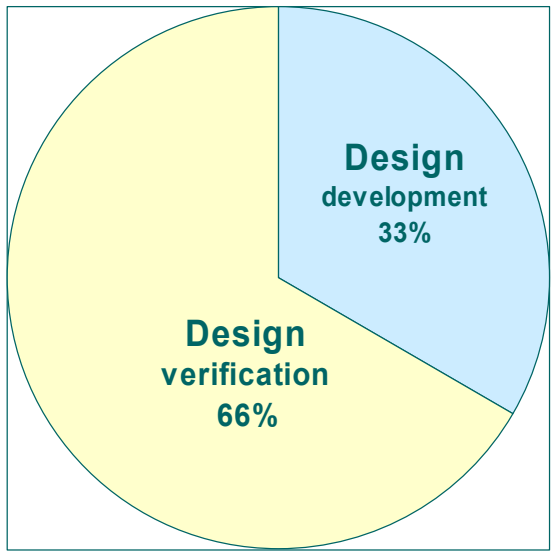
Actuality of digital systems testing

For multi-million gate ASICs, reusable Intellectual Property (IP), and System-on-Chip (SoC) designs, **verification consumes 70% of the design effort**. The number of verification engineers is usually twice the number of RTL designers. **The test bench's code makes up to 80 % of the total design code volume.**

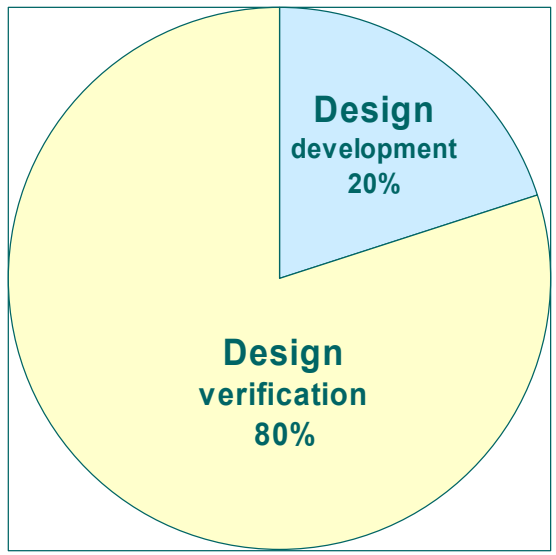
Design effort



Number of engineers

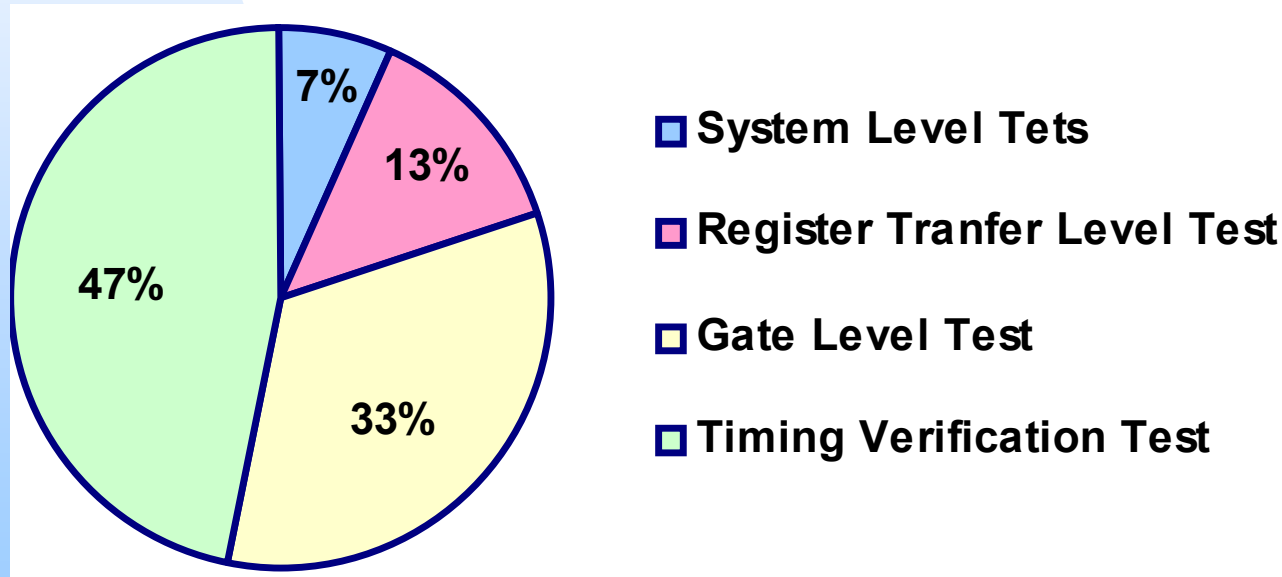


Code of design



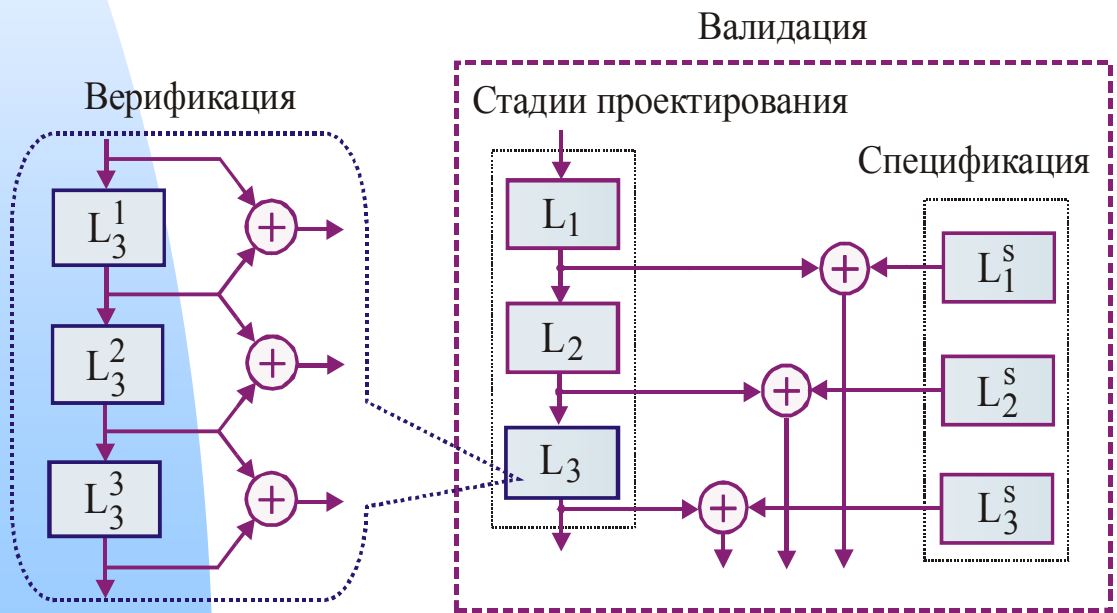
Verification costs

- On the system level compatibility of components has to be checked;
- On RT level – testing of the correctness of IP-cores (black boxes) functionality and interconnections;
- On the gate level – using of stuck-at-fault model;

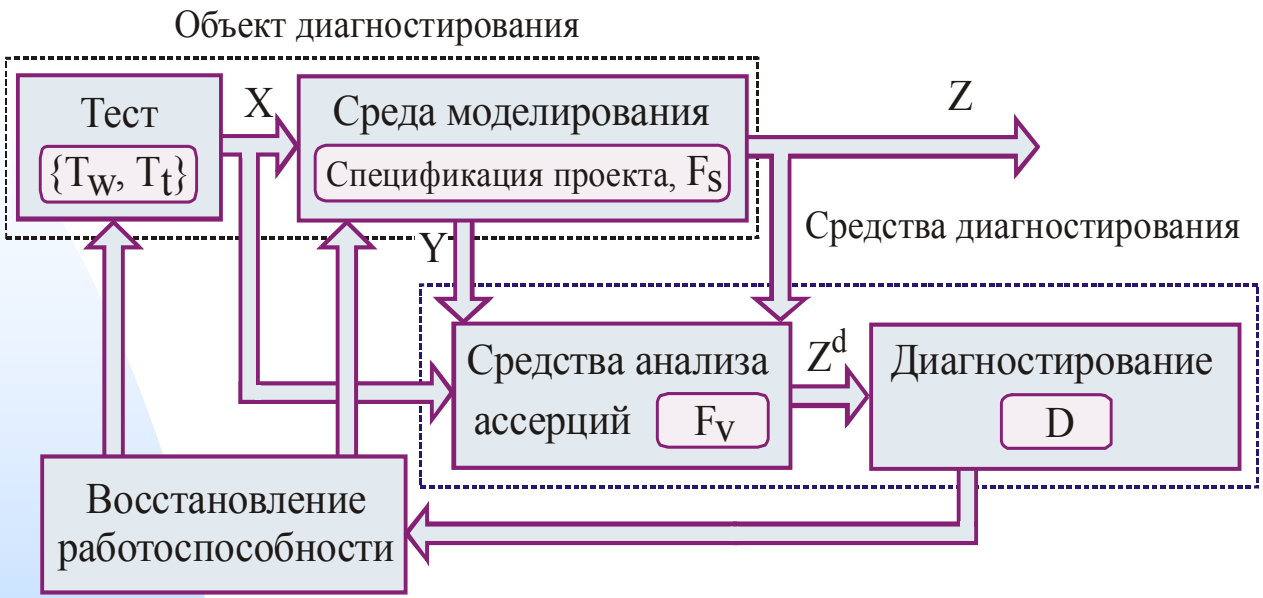


Hierarchical validation and verification

- Verification is applied to the component (phase) of design process;
- Validation is applied up to the whole (process) system.



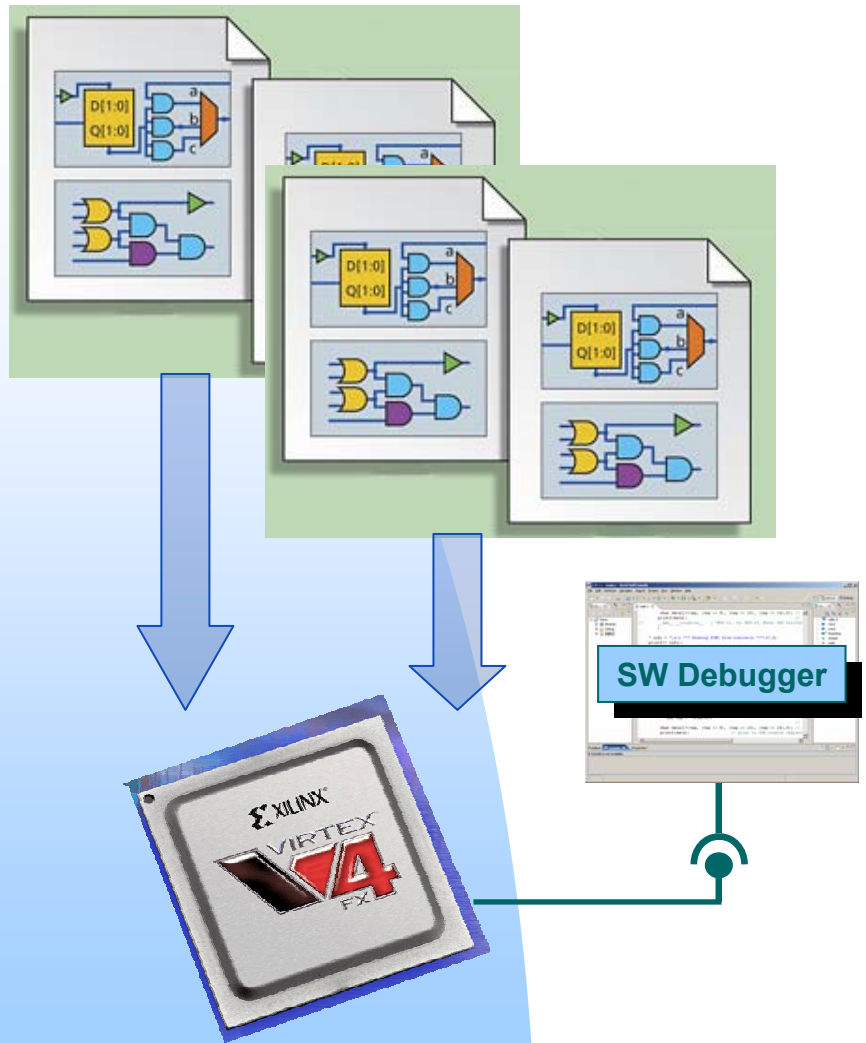
Verification model based on assertions



Computational complexity of testing and verification

$$\varphi = \frac{Q(T_t) + Q(F_s)}{Q(T_w) + Q(F_s) + Q(F_v)} \approx \frac{Q(T_t)}{Q(T_w)} \approx 3 \div 10$$

Verification in Hardware



Pros:

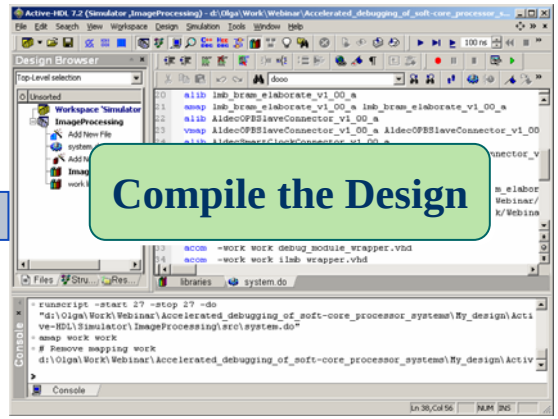
- System runs at a full speed
- Access to software is available

Cons:

- No or limited access to hardware part of the design
- External devices (logic analyzer) should be used
- Once an error is found in hardware part of the design implementation process should be run again

Accelerated Design Simulation

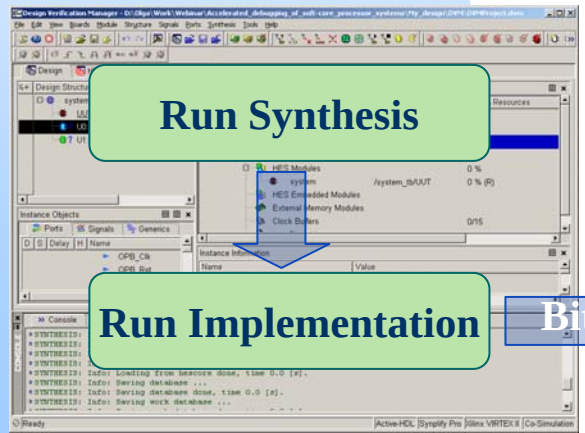
Active-HDL Simulator



Import the Design to DVM

Compile the Design

Design Verification Manager (DVM)



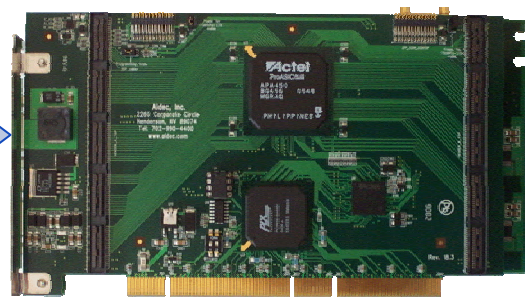
Run Synthesis

Run Implementation

Bitstream

Run co-simulation

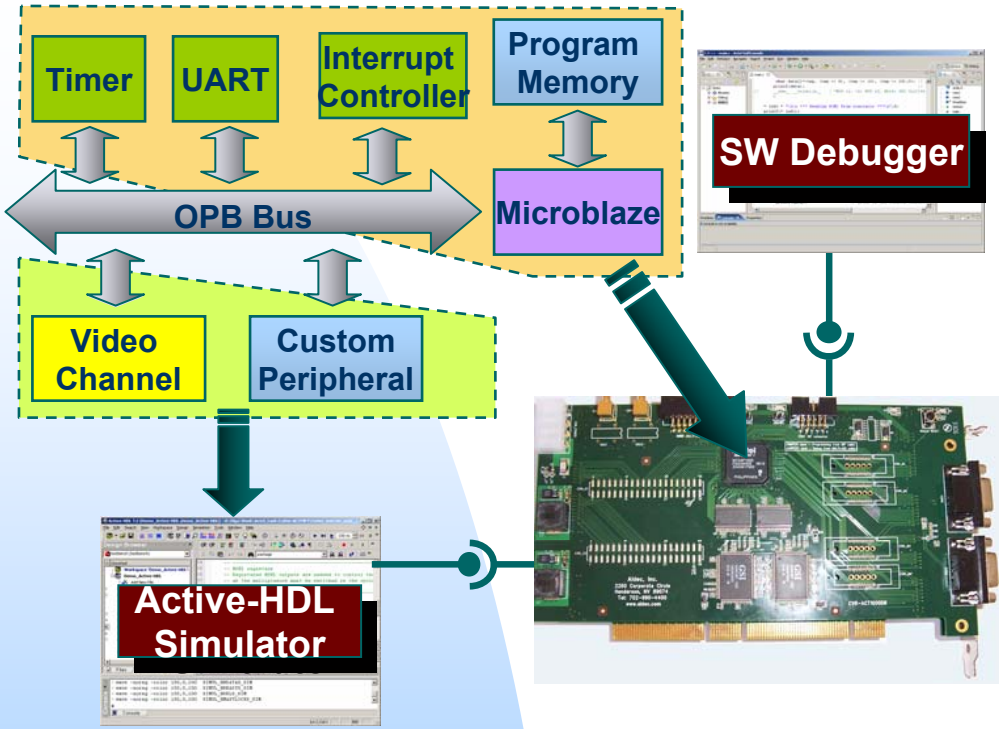
HW Board



Outline:

- The design is compiled in Active-HDL simulator
- Design is divided into 2 parts: one that should stay in simulator and one that should go to HES board
- The design runs on simulator's clock (10-100Khz)
- Testbench stays in simulator

Accelerated Design Simulation with SW debugger



Outline:

- The design is compiled in Active-HDL simulator
- Testbench stays in simulator
- The Microblaze processor as well as standard peripherals are implemented in hardware
- Custom peripherals that need to be debugged stay in simulator
- Software debugger is connected to the processor using stub
- The design runs at a hardware speed

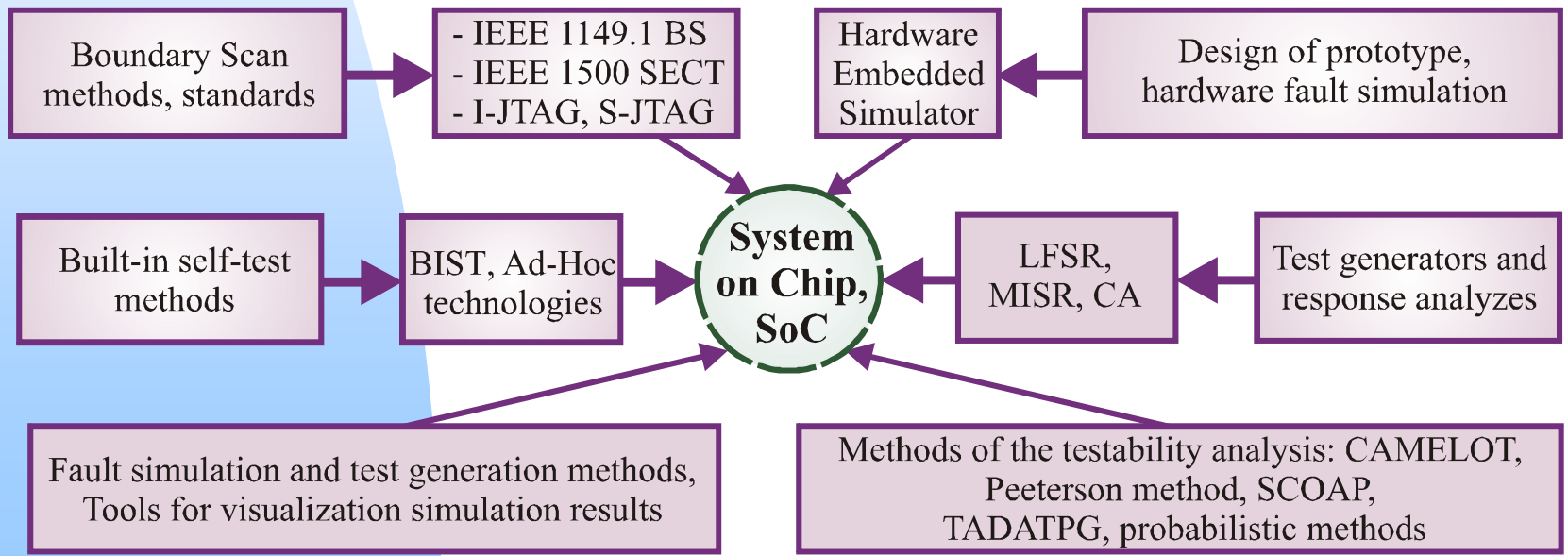
Acceleration results:

	Image Processing Design
HDL Simulation (Simulator only)	4h
Accelerated Simulation	**25 sec**

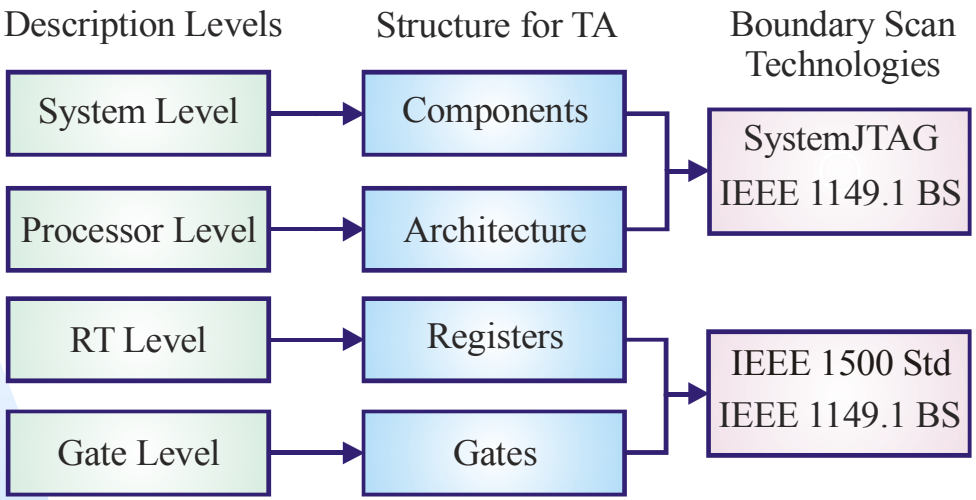
System on Chip Design

During design process, following moments have to be considered:
- testability analysis (on all design stages)
- integration DFT logic in the device (using of testable design standards),
- procedure of test generation and device testing execution.

Also, hardware simulation (HES technology) could be used instead of testability analysis and Ad-Hoc technologies.



Testability Analysis Methods and Structural Analysis of the Circuit



Developed methods for different level of abstraction could be used on the device structure before synthesis (circuit, described on hardware description languages), on register transfer level (post synthesis structure), gate level.

Practical significance and advantages are:

1) Arising of quality of faults covering (10-30 %) of existing test with small hardware-controlled expenditures (up to 20 %).
2) Time decreasing of tests synthesis by separation of testing and functional procedures.
3) Spending of device analysis on the earliest design stages and increasing of Yield Ration.

Projects in Education

- OpenTEST - *Knowledge testing computer system*
- Microsoft IT-academy
- Intel open courses on parallel programming
- Intel wireless & RFID laboratory
- Antivirus course from Kaspersky lab
- Intel + Microsoft management for diplomas topics
- Internship of 20-30 students per Year (Aldec, Intel, Microsoft, Cadence)

Internships

- **Cadence …?**
- **EchoStar**
- **Aldec, Inc.**
  - 19 students passed internship in 2006;
  - 11 students obtained name grants;
  - 60 students attend Aldec courses;
- **Intel**
  - 3 students successfully passed internship;
- **Microsoft**
  - 4 students successfully passed trainings and obtained diplomas;
- **Kaspersky Antivirus Lab**
  - 2 teachers successfully passed trainings and obtained diplomas;

Club Education is our brand

Partnership:

Microsoft (MS IT-academy), Intel, Cadence, Aldec, Kaspersky Lab, Freecode, Echostar, Softline, Mentor Graphics, Synopsys, IIT, ADB.

- **Courses from companies:**
- .NET/C# programming, SQL Server, ASP.NET
- Microsoft Solutions Framework
- Multicore and parallel programming
- Computer viruses and tools for viruses control
- Hardware/Software design and testing
- Hardware description language VHDL/Verilog/SystemC
- Information Technology Infrastructure Library (ITIL)
- **Creation of the technological corporative institutes as University subdivisions.**

Essence of Club Education

There is system of additional optional students activity, which directed to knowledge obtaining in the high-technology field.

Club education includes:

- lectures of the best world scientists in Hardware/Software Technology;
- lectures of the best world scientists in English;
- weekly seminars;
- scientists projects, grants;
- English movie;
- Conferences organization;
- Best conferences participation in area of computer and program engineering;
- trainings and probation in foreign universities, sport and active rest.

For club education new laboratory have been created, which works with the following direction: Hardware/Software Design and Test, RFID and Wireless, Networks Management, Soc and NoC Design, Image and Data Compression, Security and Antivirus, Parallel Programming.

Technological corporative institute

• Agreements between University and world leader companies (Microsoft, Intel, Cadence, Aldec, Kaspersky Lab, Freecode, Echostar, Softline, Mentor Graphics, Synopsys);

• Students recruitment into target group, beginning from second grade level, conduct a three-power treaty **(Student – Company – University);**

• Students grants from Company (100 USD);

• Additional teacher scholarship for technological courses for company (300 USD).

• Educational courses from companies for university, technological equipment and practice bases for specialists training.

5th IEEE East-West Design & Test Symposium

- **By 2006 year meeting results, workshop has been changed to Symposium – Armenia, Yerevan, 2007**

- Number of participants: 103, number of countries: 27
- The first EWDT Workshop was held in September, 2003;
- Participants from over 29 countries have attended the Workshop since 2003;
- The workshop is 100% sponsored by IEEE Computer Society
- organized in cooperation with:
  - Tallinn University of Technology
  - Moscow Institute of Control Sciences

  Sponsorship by
  - Aldec Inc
  - Intel
  - Microsoft
  - Cadence - ?
  - Synopsys
  - Echostar
  - Mentor Graphics
  - IBM
  - (Wladek Grabinski, MOS-AK Workshop)
- In 2004, 2005 the Workshop was awarded with IEEE International Recognition Awards.
- Five diplomas from IEEE Computer Society (Vladimir Hahanov, Svetlana Chumachenko, Olga Melnikova, Maryna Kaminska, Volodymyr Obrizan)

Aldec–KNURE 8 years

- 23 years on EDA market
- Headquarters in Nevada, US
- R&D center in Poland, new in Ukraine
- > 3000 corporate clients
- > 1500 university programs that involve Aldec tools

Aldec Clients:

RENESAS Everywhere you imagine.

U.S. DEPARTMENT OF DEFENSE

TOSHIBA

NASA National Aeronautics and Space Administration

BOEING

Raytheon

Rockwell Automation

Aldec Partners:

STARC

ALTERA

Actel

XILINX

ATMEL

Synplicity Simply Better Results

Lattice Semiconductor Corporation

EchoStar+KhNURE

Technologies for education in area of high definition digital television: Certified courses, themes for course projects, diplomas, PhDs; Books, Certified software, Special equipment.

For students: Scholarship for the best students of University oriented for working in EchoStar.

For teachers: Additional salary for courses, devoted to EchoStar technologies.

For the EWDT Symposium: sponsorship, supporting the best students and professors reports in areas of Design and Test.

Research and Development: projects, devoted to software/hardware (RF, analog, SoC) design and testing.

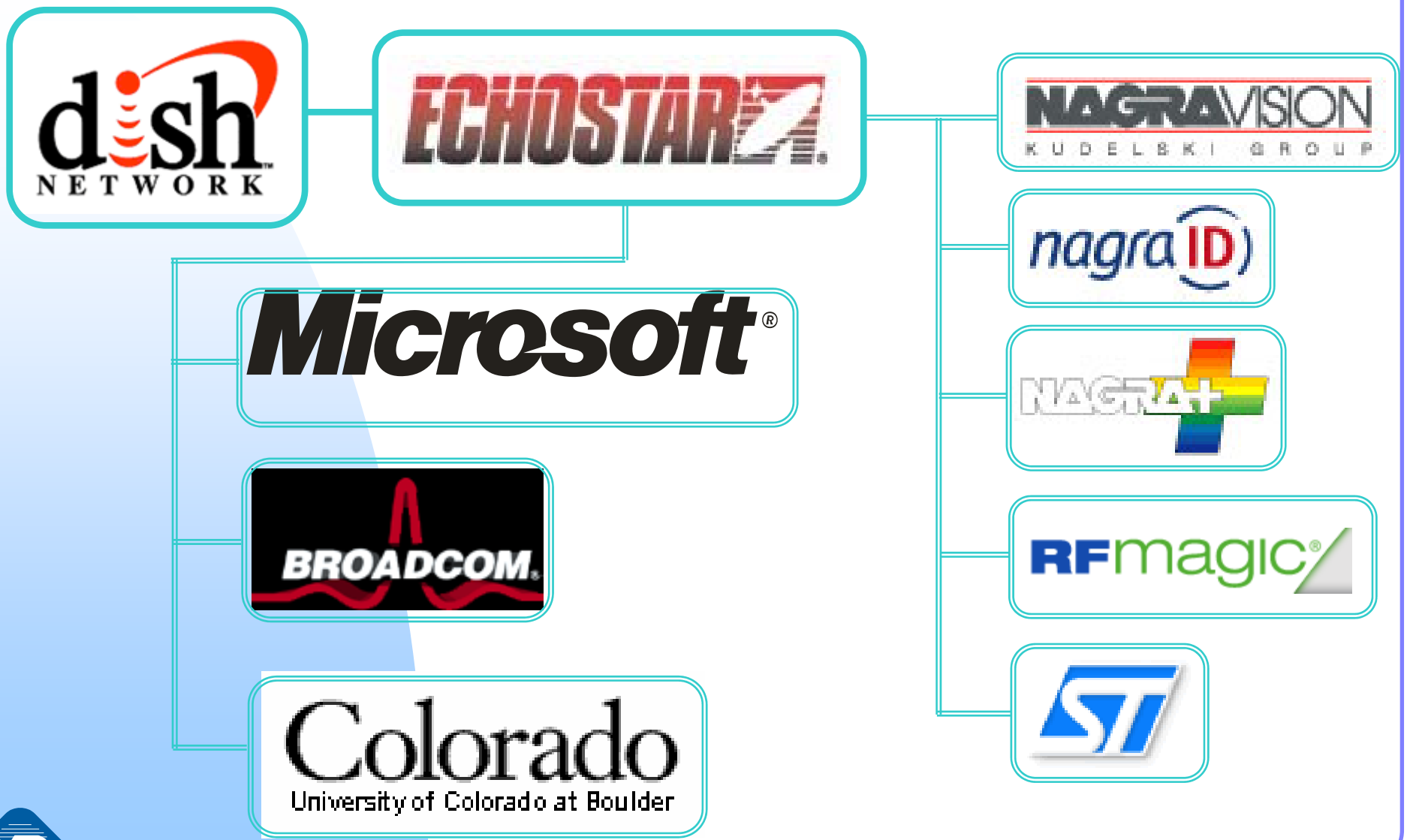
Business: what EchoStar is waiting from University - establishing EchoStar Ukraine, recruiting 50 engineers and students from our University, others University from Kharkov, Ukraine.

Support in part of furniture, computer equipment, advertising (TV, newspapers, journals, magazines), promotion of high-definition digital television in Ukraine.

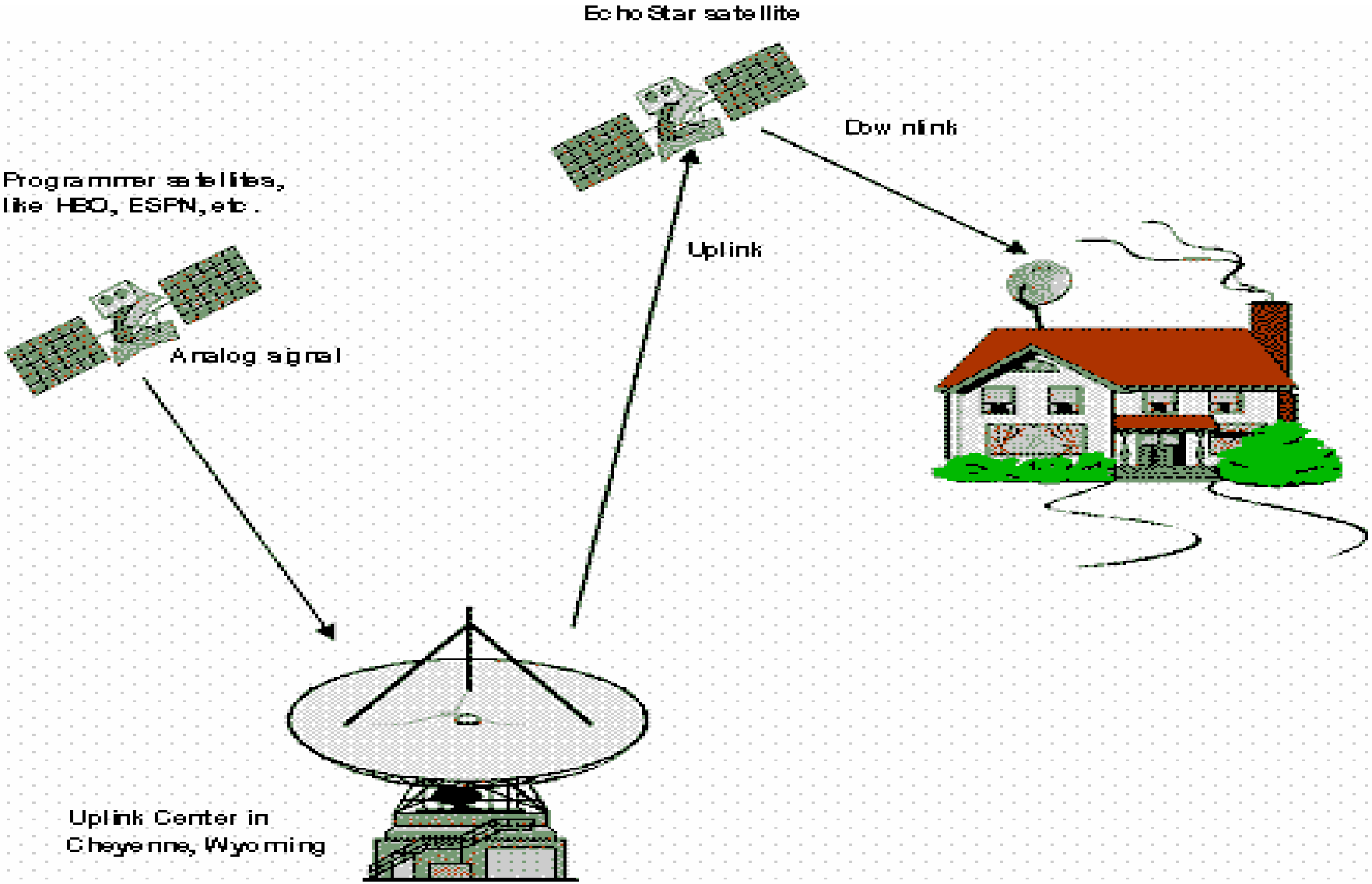
Echostar products

- **DISH 311** – High volume single tuner standard satellite receiver;
- **DISH 322** – Dual-Tuner Receiver that supports two TVs with independent programming;
- **DISH Player-DVR 625** – Dual-tuner, Dual-TV DVR receiver;
- **ViP211** – MPEG4 Single-tuner HD receiver;
- **ViP222** – MPEG4 Dual-tuner, Dual-TV HD receiver;
- **ViP622** – MPEG4 Dual-tuner, Dual-TV HD DVR receiver;
- **Pocket DISH™** – Portable Playback Device which records programming from DISH Network receivers via USB;

Echostar partnership



Satellite Basics

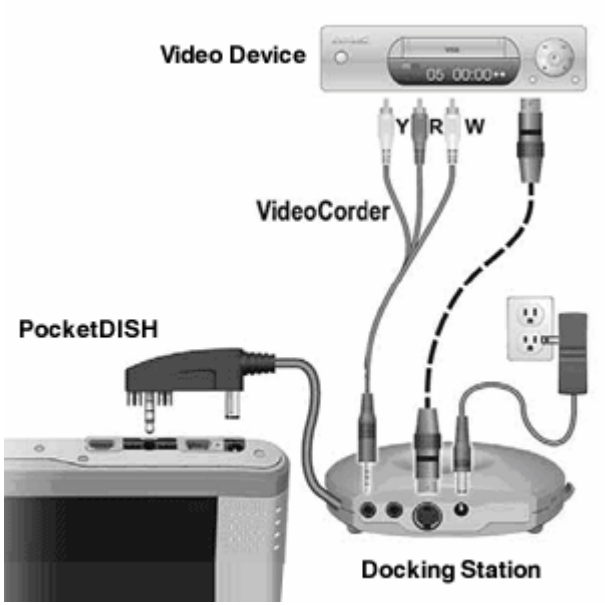


HDTV Home

DVR (Digital Video Recorder)

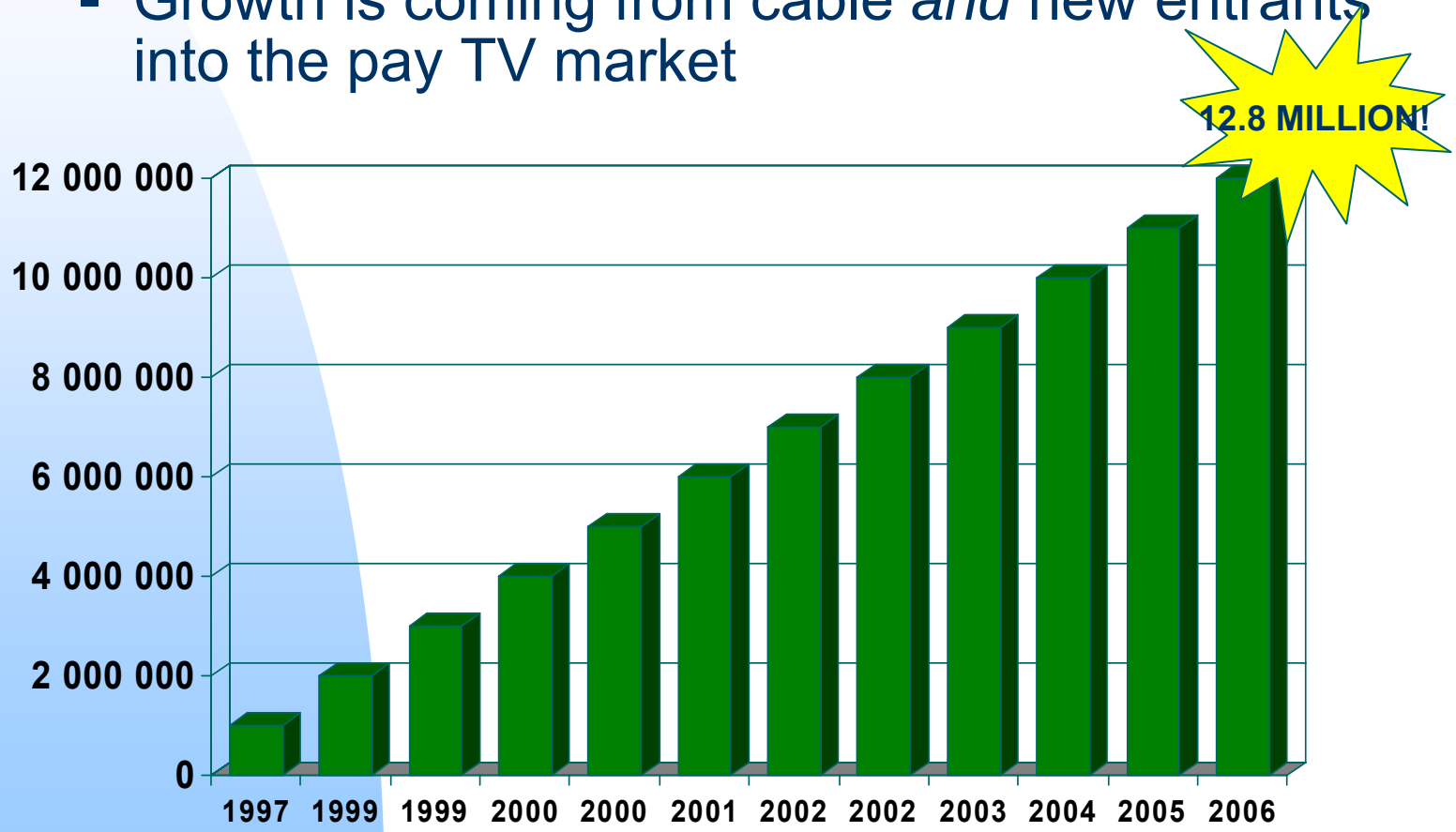
- DISH Player-DVR 942 HDTV Information:
  - The DISH Player-DVR 942 is a true two-tuner full-featured satellite receiver, which allows reception of both standard definition (SD) and high definition (HD) DISH Network programming and allows recording to a built-in hard drive. It also has a built in 8VSB Tuner for off-air digital programming. The 942 satellite receiver delivers local off-air analog and digital HDTV programming (where available), in addition to the standard and high definition DISH Network digital satellite programming already supported. The 942 receiver also supports 8PSK for additional DISH Network HDTV content. It can record up to 25 hours of HD content.
- DISH Player-DVR 921 HDTV Information:
  - The DISH Player-DVR 921 is a full-featured satellite receiver, which allows reception of both standard definition (SD) and high definition (HD) DISH Network programming and allows recording to a built-in hard drive. It also has a built in 8VSB Tuner for off-air digital programming. The 921 satellite receiver delivers local off-air analog and digital HDTV programming (where available), in addition to the standard and high definition DISH Network digital satellite programming already supported. The 921 receiver also supports 8PSK for additional DISH Network HDTV content. It can record up to 25 hours of HD content. Only one set of outputs is active at a time (either HD or SD).

Digital Video



Phenomenal Growth Continues

- Despite the competitive forces, DBS continues to take market share from cable
- Growth is coming from cable *and* new entrants into the pay TV market



Broadcom company

Broadcom Corporation is a global leader in semiconductors for wired and wireless communications. Our products enable the delivery of voice, video, data and multimedia to and throughout the home, the office and the mobile environment. Broadcom provides the industry's broadest portfolio of state-of-the-art system-on-a-chip and software solutions to manufacturers of computing and networking equipment, digital entertainment and broadband access products, and mobile devices. These solutions support our core mission: Connecting everything.

Broadcom, one of the world's largest fabless semiconductor companies with annual revenue of more than $2.5 billion, is headquartered in Irvine, Calif., and has offices and research facilities in North America, Asia and Europe.

Proprietary communications systems algorithms and protocols;

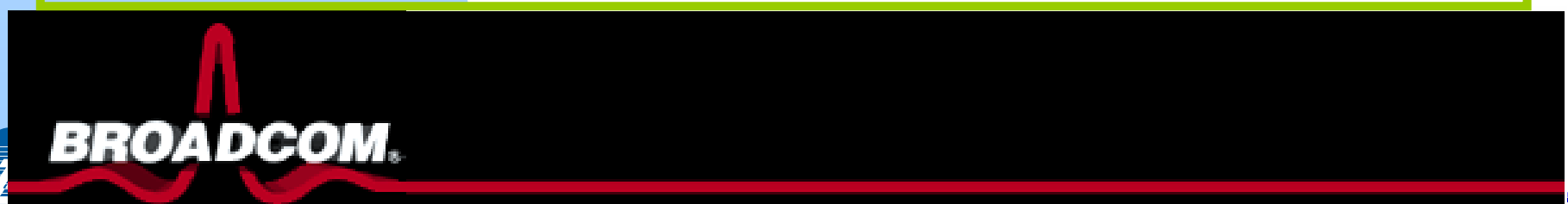
Advanced DSP hardware architectures;

System-on-a-chip design methodologies and advanced library development for both standard cell and full-custom integrated circuit design;

High-performance radio frequency, analog and mixed-signal circuit design using industry-standard CMOS processes;

High-performance custom microprocessor architectures and circuit designs;

Extensive software reference platforms to enable complete system-level solutions



RF MAGIC COMPANY

RF Magic is a fabless semiconductor company providing a diversified portfolio of radio frequency (RF) Systems on a Chip integrated circuits (ICs) for the next generation of consumer electronics applications. The company's experienced engineers combine RF and digital communications systems experience with RF silicon design expertise to develop highly advanced ICs for cost-effective integration into high-volume consumer platforms.

RFmagic®

STMicroelectronics COMPANY

STMicroelectronics

ST is one of the world's largest semiconductor companies, with net revenues of US$9.85 billion in 2006 and market leadership that is spread across many fields. For example, according to the latest industry data, ST is the world's fifth largest semiconductor company and has leading positions in sales of Analog Products, Analog Application Specific Integrated Circuits and Analog Application Specific Standard Products.

ST is also number one in camera modules for mobile phones, number two in discretes and analog, and number three in NOR Flash, as well as in the application segments of Automotive, Industrial, and Wireless. ST is also the leading supplier of semiconductors for set-top boxes and power management devices. Furthermore, ST was the 3rd biggest semiconductor supplier in China in 2005.

NAGRAVISION

A world leader for conditional access systems

Nagravision is a market leader in the field of conditional access for digital TV and broadband Internet. Leading operators are equipped with its technology which ensures secure access to their services via more than 40 million decoders (analog and digital).

The range of Nagravision solutions includes systems for:

- security of access to information - for the operator (encryption and access rights management) and for the end-user (decryption through the decoder/smart card pair)
- content and subscriber management
- management and security for interactivity over IP networks

Выводы. 1

1. Американские фирмы не имеют приоритетов для Hiring в Индии или Китае, если наши студенты знают английский язык.
2. Американские фирмы готовы инвестировать средства для образования компаний в Украине. Менее интересными становятся outsourcing отношения как для них, так и для нас, поскольку практически отсутствует приток высоких технологий в страну.
3. Бизнес-модель: производить продукт здесь, а продавать его там (США) – выгодна для нас (рабочие места, высокие зарплаты, конкуренция на рынке труда с локальной индустрией) и для них (в 5 – 10 раз более низкая зарплата).
4. Перспективным выходом на мировой рынок является – влиться в технологический процесс брендовой компании – менеджмент от них, технологии от них, сегмент рынка их, наш продукт как модификация их технологий.
5. Американские граждане не хотят быть инженерами, технологами, но менеджерами и бизнесменами. Это есть шанс для наших вузов готовить классных специалистов, но получив при этом их технологии, технику и лицензионные продукты.

Выводы. 2

6. Университеты должны становиться корпоративными: получать финансовую, технологическую, техническую помощь от глобальной и локальной индустрии. Компании должны контролировать и вносить изменения в образовательные процессы университетов через корпоративные наблюдательные советы. Университет Колорадо, например, не имеет права изменять курсы и учебные планы без согласования с наблюдательным советом.
7. Все более многочисленными становятся предложения от брендов в части Hardware Design and Testing (Echostar, ST, RF Magic, Nagra, Broadcom). Следовательно, необходимо внедрять в учебный процесс технологии от ведущих фирм в области EDA (Cadence, Mentor Graphics, Synopsis, Magma).
8. Цифровое телевидение со стороны Echostar интересно для Украины не только как центр проектирования и тестирования программного обеспечения, но и как обреченный на успех бизнес-проект, интересный для локальных инвесторов, потребителей бренда high definition digital satellite TV (до 1 000 000 потенциальных пользователей в течение 5 последующих лет).
9. Стоимость проекта – 300 000 000 долларов – вполне посильная для 10 – 20 частных инвесторов из Украины и России. Сейчас в США более 500 цифровых каналов и 31 канал высокой разрешающей способности. Это должно быть и будет в Украине. 3 российских сателлита

Выводы. 3

10. Компаниям интересны не отдельные умные студенты-выпускники, но мобильные группы специалистов, организованные в команду с сильными лидерами. Клубы по интересам способны подготовить такие команды по различным технологическим направлениям, которые заточены под конкретные глобальные и/или локальные фирмы.
11. Наш университет и факультет Компьютерной инженерии не только открыт, но и активен в части ежегодного обновления курсов от ведущих компаний мира, а также от локальной индустрии. Сегодня мы имеем клубы (курсы) от Microsoft, Intel, Kaspersky lab, Aldec, FreeCode.
12. Курсы от университетов: Таллинна, Беркли, Турина, Денвера, Варшавы.
13. Центры компетенции:
    1) по вычислительных архитектурам от Евросоюза.
    2) по параллельным вычислениям, беспроводным технологиям и робототехнике при поддержке Intel к концу мая 2007 года.
    3) satellite HDTV технологий от компании Echostar – конец лета.
    4) for Electronic Design Automation from Cadence – our white dream!
14. Приход производителей высокотехнологичной аппаратуры на рынок Украины дает дополнительный стимул для активизации деятельности бренда Cadence и среди университетов в первую очередь!

Patric Gelsinger – Vice-president, Intel, San Diego

Eric Rudder – Microsoft Vice-President awarded diploma from KNURE students, Kiev

Cadence: Jury Kaufhold, ….